AMENDMENT TO THE CLAIMS

Please replace the presently pending claims as follows:

1. (Currently Amended) A circuit having:

an input for receiving an input signal containing a plurality of bits at an input frequency and for receiving a representation of desired output frequency;

a splitter, which splits ~~for splitting~~ the input signal into a plurality of split signals each at a frequency of the desired output frequency;

a plurality of catchers, ~~for identifying valid bits of a respective split signal~~wherein each catcher provides bits of a respective split signal and a valid signal identifying bits of the respective split signal that are valid;

a first shifter, which shifts ~~for shifting~~ valid bits of the respective split signal that are identified by at least some of the catchers by a predetermined number, and a second shifter, which shifts the valid signal identified by at least some of the catchers by the predetermined number; and

an output responsive to the shifted valid bits to provide an output signal containing a plurality of valid bits of the input signal at the desired output frequency.

2. (Original) The circuit of claim 1, wherein the output is further responsive to the shifted valid bits to derive the predetermined number.

3. (Canceled)

4. (Currently Amended) The circuit of ~~claim 3~~ claim 1, wherein the output is further responsive to the shifted valid bits to derive the predetermined number.

5. (Original) The circuit of claim 1 operating as a phase shifter, wherein the predetermined number is 1.

6. (Original) The circuit of claim 1 operating as a frequency reducer, wherein the predetermined number is greater than 1 and identifies a width of the output signal.

7. (Original) The circuit of claim 1, wherein the number of split signals and the number of catchers are based on an empirically-derived split factor.

8. (Original) The circuit of claim 7, wherein the split factor is based on the input frequency and the desired output frequency.

9. (Currently Amended) A computer useable medium having a computer readable program embodied therein for addressing data to convert a high frequency data stream to a low frequency data stream at a desired output frequency, the computer readable program comprising:

first computer readable program code for causing the computer to split the high frequency data stream into a plurality of split signals each at a frequency of the desired output frequency;

second computer readable program code for causing the ~~computer to identify valid bits of a respective split signal~~ to provide bits of a respective split signal and a valid signal identifying bits of the respective split signal that are valid;

third computer readable program code for causing the computer to shift identified valid bits of the respective split signal by a predetermined number; ~~and~~

fourth computer readable program code for causing the computer to output an output data stream containing a plurality of valid bits of the input signal at the desired output frequency; and

fifth computer readable program code for causing the computer to shift the valid signal by the predetermined number.

10. (Original) The computer useable medium of claim 9, wherein the fourth computer readable program code is further responsive to the shifted valid bits to derive the predetermined number.

11. (Canceled)

12. (Currently Amended) The computer useable medium of ~~claim 11~~ claim 9, wherein the fourth computer readable program code is further responsive to the shifted valid bits to derive the predetermined number.

13. (Original) The computer useable medium of claim 9, wherein the number of split signals is based on an empirically-derived split factor.

14. (Original) The computer useable medium of claim 13, wherein the split factor is based on the input frequency and the desired output frequency.

15. (Currently Amended) A process of converting a phase or frequency of an input data stream to desired output phase or frequency comprising:

splitting the input data stream into a plurality of split signals each at a frequency of the desired output frequency;

~~identifying valid bits of a respective split signal~~ providing a valid signal identifying bits of the respective split signal that are valid;

shifting ~~identified valid bits by a predetermined number~~ valid bits of the respective split signal by a predetermined number, and shifting the valid signal by the predetermined number; and

outputting an output data stream containing a plurality of the valid bits of the input signal at the desired output frequency.

16. (Original) The process claim 15, further including

deriving the predetermined number from the shifted valid bits.

17. (Canceled)

18. (Original) The process of claim 15, wherein the number of split signals is based on an empirically-derived split factor.

19. (Original) The process of claim 18, wherein the split factor is based on the input frequency and the desired output frequency.

20. (Original) The process of claim 15, further including

selecting a predetermined number to selectively reduce the frequency of the input data stream to an output data stream having a width based on the predetermined number or to shift a phase of the input data stream to the output data stream.